	Typ	Hits	Search Text	DBs	Time Stamp	Comments	Error Definition
1	BRS	13178	(sac or (self adj aligned adj contact))	USPAT; US-PGPUB	2003/05/28 14:23		
2	BRS	6408	((sac or (self adj aligned adj contact))) and (opening or hole or recess or trench)	USPAT; US-PGPUB	2003/05/28 14:24		
3	BRS	2667	(((sac or (self adj aligned adj contact))) and (opening or hole or recess or trench)) and (gate or electrode)	USPAT; US-PGPUB	2003/05/28 14:24		
4	BRS	1378	((((sac or (self adj aligned adj contact))) and (opening or hole or recess or trench)) and (gate or electrode)) and plurality	USPAT; US-PGPUB	2003/05/28 14:24		
5	BRS	1218	(((((sac or (self adj aligned adj contact))) and (opening or hole or recess or trench)) and (gate or electrode)) and plurality) and (source or drain)	USPAT; US-PGPUB	2003/05/28 14:24		
6	BRS	749	((((((sac or (self adj aligned adj contact))) and (opening or hole or recess or trench)) and (gate or electrode)) and plurality) and (source or drain)) and (isolation or (field adj oxide))	USPAT; US-PGPUB	2003/05/28 14:25		
7	BRS	605	(((((((sac or (self adj aligned adj contact))) and (opening or hole or recess or trench)) and (gate or electrode)) and plurality) and (source or drain)) and (isolation or (field adj oxide))) and @ad<=20010813	USPAT; US-PGPUB	2003/05/28 15:20		

	U	1 [1]	Document ID	Issue Date	Pag s	Title	Current OR	Current XRef	R trieval Classif
1	☐	☒	US 20030023174 A1	20030130	12	Medical testing system with an illuminating component and automatic shut-off	600/508		
2	☐	☒	US 20030013253 A1	20030116	11	Optimized flash memory cell	438/257	438/258	
3	☐	☒	US 20030011023 A1	20030116	11	Metal local interconnect self-aligned source flash cell	257/315	257/316; 438/201; 438/257; 438/626; 438/627	
4	☐	☒	US 20020140008 A1	20021003	38	Semiconductor device and its manufacture	257/288		
5	☐	☒	US 20020111006 A1	20020815	10	Method for forming landing pad	438/612		
6	☐	☒	US 20020070398 A1	20020613	37	SEMICONDUCTOR MEMORY DEVICE USING DOUBLE LAYERED CAPPINGPATTERN AND SEMICONDUCTOR MEMORY DEVICE FORMED THEREBY	257/296		
7	☐	☒	US 20020025669 A1	20020228	21	Methods of forming a contact structure in a semiconductor device	438/637		
8	☐	☒	US 20010019142 A1	20010906	71	SEMICONDUCTOR DEVICE AND METHOD OF FABRICATING THE SAME	257/296		
9	☐	☒	US 20010005626 A1	20010628	11	Method for fabricating semiconductor device	438/637		

	Inv ntor	S	C	P	2	3	4	5	Imag Doc. Display d	PT
1	Surwillo, John M. et al.	☒	☐	☐	☐	☐	☐	☐	US 20030023174	☐
2	Hurley, Kelly T.	☒	☐	☐	☐	☐	☐	☐	US 20030013253	☐
3	Hurley, Kelly T.	☒	☐	☐	☐	☐	☐	☐	US 20030011023	☐
4	Yasuda, Makoto	☒	☐	☐	☐	☐	☐	☐	US 20020140008	☐
5	Wu, King-Lung et al.	☒	☐	☐	☐	☐	☐	☐	US 20020111006	☐
6	Lee, Jae-Goo	☒	☐	☐	☐	☐	☐	☐	US 20020070398	☐
7	Hwang, Min-Wk et al.	☒	☐	☐	☐	☐	☐	☐	US 20020025669	☐
8	NAKAHATA, TAKUMI et al.	☒	☐	☐	☐	☐	☐	☐	US 20010019142	☐
9	Kim, Jeong Ho et al.	☒	☐	☐	☐	☐	☐	☐	US 20010005626	☐

	U	1 [1]	Document ID	Issue Dat	Pages	Titl	Current OR	Current XRef	Retrieval Classif
10	☐	☒	US 6534375 B2	20030318	150	METHOD OF FORMING A CAPACITOR IN A SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE USING A METAL SILICON NITRIDE LAYER TO PROTECT AN UNDERLYING METAL SILICIDE LAYER FROM OXIDATION DURING SUBSEQUENT PROCESSING STEPS	438/386	438/387; 438/399; 438/683; 438/686; 438/785	
11	☐	☒	US 6465310 B2	20021015	8	Methods of forming self-aligned contact pads on electrically conductive lines	438/299	438/229	
12	☐	☒	US 6461923 B1	20021008	10	Sidewall spacer etch process for improved silicide formation	438/305	438/586; 438/680	
13	☐	☒	US 6437411 B1	20020820	35	Semiconductor device having chamfered silicide layer and method for manufacturing the same	257/413	257/316	
14	☐	☒	US 6432816 B1	20020813	10	Method for fabricating semiconductor device	438/637	438/299	
15	☐	☒	US 6417097 B1	20020709	21	Methods of forming a contact structure in a semiconductor device	438/637	438/773; 438/783	
16	☐	☒	US 6352896 B1	20020305	29	Method of manufacturing DRAM capacitor	438/253	438/396; 438/672; 438/675	
17	☐	☒	US 6350650 B1	20020226	22	Method for fabricating a semiconductor memory device	438/256	438/240	
18	☐	☒	US 6342416 B1	20020129	28	Method of manufacturing a semiconductor memory device	438/239	438/238; 438/626; 438/761	

	Inventor	S	C	P	2	3	4	5	Image Doc. Display d	PT
10	Iijima, Shinpei et al.	☒	☐	☐	☐	☐	☐	☐	US 6534375	☐
11	Lee, Jae-Goo et al.	☒	☐	☐	☐	☐	☐	☐	US 6465310	☐
12	Hui, Angela T. et al.	☒	☐	☐	☐	☐	☐	☐	US 6461923	☐
13	Choi, Chang-won et al.	☒	☐	☐	☐	☐	☐	☐	US 6437411	☐
14	Kim, Jeong Ho et al.	☒	☐	☐	☐	☐	☐	☐	US 6432816	☐
15	Hwang, Min-Wk et al.	☒	☐	☐	☐	☐	☐	☐	US 6417097	☐
16	Liu, Haochieh et al.	☒	☐	☐	☐	☐	☐	☐	US 6352896	☐
17	Lee, Pyung Woo	☒	☐	☐	☐	☐	☐	☐	US 6350650	☐
18	Kim, Ji-soo et al.	☒	☐	☐	☐	☐	☐	☐	US 6342416	☐

	U	1 [1]	Document ID	Issue Date	Pag s	Title	Current OR	Current XRef	Retrieval Classif
19	☐	☒	US 6303430 B1	20011016	13	Method of manufacturing DRAM capacitor	438/253	257/E21.019; 438/254; 438/255; 438/396; 438/397; 438/398	
20	☐	☒	US 6271081 B1	20010807	49	Semiconductor memory device	438/243	257/E21.653; 438/248; 438/268; 438/386; 438/982	
21	☐	☒	US 6248654 B1	20010619	16	Method for forming self-aligned contact	438/597	257/E21.507; 438/261; 438/263	
22	☐	☒	US 6172898 B1	20010109	49	Semiconductor memory device	365/149	257/301; 257/E21.653; 365/63	
23	☐	☒	US 6080624 A	20000627	27	Nonvolatile semiconductor memory and method for manufacturing the same	438/257	257/E21.682; 257/E27.103; 438/585	
24	☐	☒	US 5858833 A	19990112	14	Methods for manufacturing integrated circuit memory devices including trench buried bit lines	438/253	257/E21.648; 257/E27.086; 438/244; 438/633	

	Inventor	S	C	P	2	3	4	5	Imag Doc. Displayed	PT
19	Jenq, J. S. Jason	☒	☐	☐	☐	☐	☐	☐	US 6303430	☐
20	Kajiyama, Takeshi	☒	☐	☐	☐	☐	☐	☐	US 6271081	☐
21	Lee, Joo-Young et al.	☒	☐	☐	☐	☐	☐	☐	US 6248654	☐
22	Kajiyama, Takeshi	☒	☐	☐	☐	☐	☐	☐	US 6172898	☐
23	Kamiya, Eiji et al.	☒	☐	☐	☐	☐	☐	☐	US 6080624	☐
24	Lee, Won-seong et al.	☒	☐	☐	☐	☐	☐	☐	US 5858833	☐